S/N 10/749901 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

plicant: Gregory M. Chrysler et al.

Examiner:

Unknown

2 9 2004 Serial No.:

10/749901

Group Art Unit:

2811

Fried:

December 29, 2003

Docket:

884.A74US1

Title:

INTEGRATED MICRO CHANNELS AND MANIFOLD/PLENUM USING

SEPARATE SILICON OR LOW COST POLYCRYSTALLINE SILICON

Assignee:

Intel Corporation

Customer No:

21186

INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Information Disclosure Statement considered.

INFORMATION DISCLOSURE STATEMENT

Serial No: 10/749901

Filing Date: December 29, 2003

Title: INTEGRATED MICRO CHANNELS AND MANIFOLD/PLENUM USING SEPARATE SILICON OR LOW COST

POLYCRYSTALLINE SILICON

Assignee: Intel Corporation

The present application is either a U.S. national patent application filed after June 30, 2003 or an international application that entered the national stage under 35 U.S.C. § 371 after June 30, 2003. Thus, Applicant believes that the U.S. Patent & Trademark Office has waived the requirement under 37 C.F.R. 1.98 (a)(2)(i) for submitting a copy of each cited U.S. patent and each U.S. patent application publication. The waiver is provided in a pre-OG notice from the U.S. Patent & Trademark Office entitled "Information Disclosure Statements May Be Filed Without Copies of U.S. Patents and Published Applications in Patent Applications filed after June 30, 2003" and dated July 11, 2003. Applicant acknowledges the requirement to submit copies of foreign patent documents and non-patent literature in accordance with 37 C.F.R. 1.98(a)(2).

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

GREGORY M. CHRYSLER ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A. Attorneys for Intel Corporation

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Dkt: 884.A74US1 (INTEL)

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 2379 day of November, 2004.

N/ -----

Signature

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Substitute for form 1449A/PTO	Complete if Known		
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application Number	10/749901	
(Use as many sheets as necessary)	Filing Date	December 29, 2003	
/0\$	First Named Inventor	Chrysler, Gregory	
MOV 2 9 2004 35	Group Art Unit	2811	
	Examiner Name	Unknown	
	Attorney Docket No: 8	84.A74US1	

	US PATENT DOCUMENTS						
Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T²

	OTHE	R DOCUMENTS NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*			T²
		TUCKERMAN, D. B., et al., "High-Performance Heat Sinking for VLSI", <u>IEEE</u> <u>Electron Device Letters</u> , Vol. EDL-2, No. 5, (May 1981), 126-129	